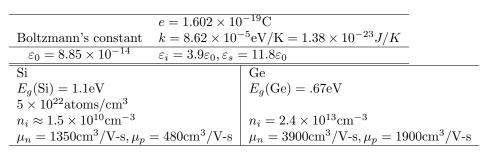
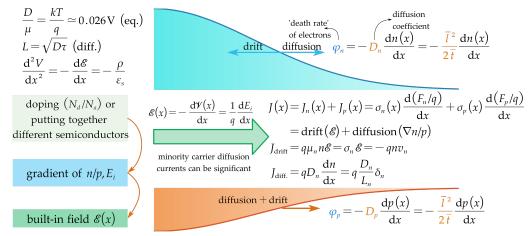
Semiconductor Final CheatSheet (chapter5-7)



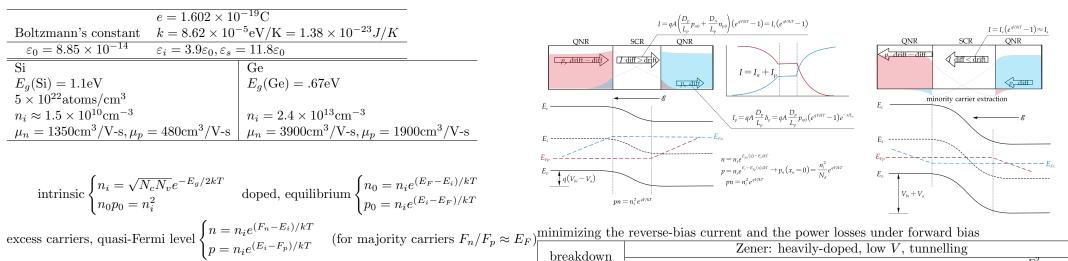
$$\text{intrinsic} \begin{cases} n_i = \sqrt{N_c N_v} e^{-E_g/2kT} \\ n_0 p_0 = n_i^2 \end{cases} \quad \text{doped, equilibrium} \begin{cases} n_0 = n_i e^{(E_F - E_i)/kT} \\ p_0 = n_i e^{(E_i - E_F)/kT} \end{cases}$$

space charge neutrality $\delta n(t) = \delta p(t)$.



Junctions

kT 1 p_p kT 1 N_qN_d		
$V_0 = \frac{kT}{q} \ln \frac{p_p}{p_n} = \frac{kT}{q} \ln \frac{N_a N_d}{n_i^2}$	junction cap.	storage charge cap.
$Q = qAx_{n0}N_d = qAx_{p0}N_a$	due to dipole	diffusion charge p_n, n_p
$W = \sqrt{\frac{2\varepsilon_s V_0}{q} \left(\frac{N_a + N_d}{N_a N_d}\right)} \mathscr{E}_{max} = -\frac{2V_0}{W}$	$C_j = \left \frac{\mathrm{d}Q}{\mathrm{d}V_R} \right = \frac{\varepsilon_s A}{W}$	$C_s, Q_p = qA \int_0^\infty \delta p_n \mathrm{d}x_n$
$x_n = W \frac{N_a}{N_a + N_d}$ $x_p = W \frac{N_d}{N_a + N_d}$	reverse-biased	forward-biased

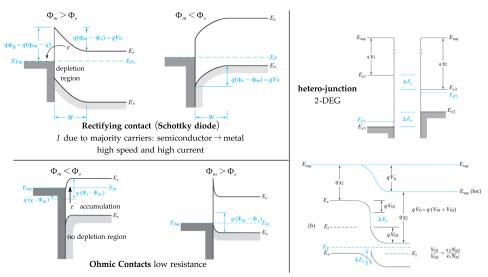


r)					
F')	breakdown	Zener: heavily-doped, low V , tunnelling			
		Avalanche: higher V, EHP multiplication, drift in SCR; $V_B = \frac{\varepsilon_s E_{crit}^2}{2eN_d}$			
	transient/ac	$i_c(t) = \frac{Q_p}{\tau_p} + \frac{\mathrm{d}Q_p}{\mathrm{d}t}, Q_p(t) = I_F \tau_p e^{-t/\tau_p}$	improve switching speed: adding		
		$v(t) = \frac{kT}{q} \ln \left(\frac{Q_p(t)}{qAL_p p_n} + 1 \right)$	recombination centers to the bulk; narrow base diode $(x_n < L_p)$		
			recombination centers to the bi		

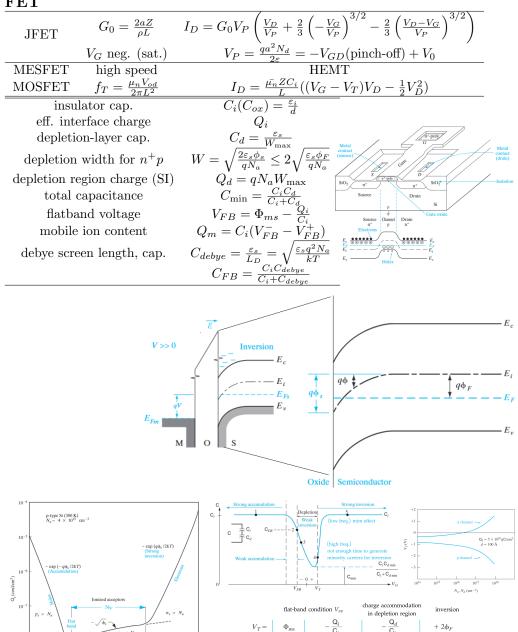
5.5.5 varactor diode

ohmic loss: For lightly doped, long diodes, resistivity of each neutral region is so high that voltage drops outside the depletion region cannot be neglected. The effects are complicated by the fact that the voltage drop depends on the current. $V = V_a - I(R_p(I) + R_n(I))$

metal-semiconductor junction



FET



(+) n channel

(+) n channel

channel length modulation	$L_{\mathrm{eff}} = L - \Delta L_{dp}(D)$
substrate bias	$\Delta V_T = rac{\sqrt{2arepsilon_s q N_a}}{C_i} (\sqrt{2\phi_F - V_B} - \sqrt{2\phi_F})$
sub-threshold	$I_D \propto (1 - e^{-qV_D/kT})e^{qV_{od}/c_rkT}$
short channel, narrow width	D&G shares Q, $L \downarrow \to V_T \downarrow, Z \downarrow \to V_T \uparrow$
gate-induced drain leakage	
drain-induced barrier lowering	before tunnelling, $I_D \uparrow$
punch-through	$DIBL \rightarrow DS$ leakage/breakdown, uncontrolled by G
gate oxide breakdown	
hot-electron	$V_T \uparrow, g_m \downarrow$

self-aligned for gate: gate as the mask for implantation of S/D

LOCal Oxidation on Si: nitride mask on gate oxide, wet oxidation, thick field oxide high k: gate oxide

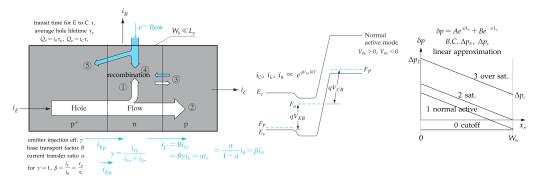
low k: field oxide (isolation)

control V_T : gate electrode, C_i , ion implantation (enhancement/depletion)

For n-type, enhancement mode: 'normally off' with zero gate voltage, $V_T > 0$ depletion mode: 'normally on' with zero gate voltage, $V_T < 0$

Lightly Doped Drain: only needed for n-channel (hot carrier; holes on valence band, low mobility)

BJT



$B = \operatorname{sech} \frac{W_b}{L_p} \approx \left(1 + \frac{1}{2} \left(\frac{W_b}{L_p^n}\right)^2\right)^{-1}$	reduce recombination: small n doping & short base width
$\gamma \approx \left(1 + \frac{n_n^B \mu_n^p W_b}{p_p^E \mu_n^p L_n^P}\right)^{-1}$	$\begin{vmatrix} \frac{n_p^E}{p_n^B} = \frac{n_n^B}{p_p^E}; \text{ doping E much higher than B,} \\ \text{hetero } E_q(E) > E_q(B) \end{vmatrix}$
$f_T = \frac{1}{2\pi au_t}$	
Early effect	B-C junction extends into B, $W_b \downarrow$, $I_C = \frac{1}{r_o}(V_{CE} + V_A)$
current crowding	at emitter edges; smaller W_b , lighter doping in B
Kirk effect	high injection of h^+ into E, $W_b \uparrow, \tau_t \uparrow, I_C \downarrow$ at high

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